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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,907	03/02/2004	Jochen Thomas	2003 P 54322 US	1415
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SLATER & MATSIL LLP 17950 PRESTON ROAD SUITE 1000 DALLAS, TX 75252			EXAMINER AU, BACH	
			ART UNIT	PAPER NUMBER
			2822	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/790,907	Applicant(s) THOMAS ET AL.	
	Examiner Bac H. Au	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 October 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 53-111 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 53-111 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 October 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on October 2, 2006, in which claims 92-111 were added, and claims 53, 59-61, 64, 66, 67, 69, 73, 78-80, 83, 85, 86, and 88 were amended, has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 53-54, 56-59, 65-66, and 68-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang (U.S. Pat. 6943294) in view of Chia (U.S. Pub. 2003/0227079).

Regarding claim 53, Kang [Fig.1] discloses a method of forming a stacked-die assembly, the method comprising:

providing a substrate [110] with contacts [125] formed on a top surface;

placing a bottom side of a first die [130₁] over the top surface of the substrate, the first die having a top side with a redistribution layer;

placing a spacer over the first die [140₁];

placing a bottom side of a second die [130₂] over the spacer, the second die having a first side with a redistribution layer; and

electrically coupling wire leads [150] from the re-routed bond pads [145] of the first die and the second die to the contacts.

Kang [Col.2 lines 36-40] discloses a redistribution layer on each die to redistribute bond pads, but fails to explicitly disclose a redistribution layer that comprises conductive lines that redistribute bond pads located on a right side and a left side of a first gap in an interior region to corresponding re-routed bond pads in a periphery region.

However, Chia [Fig.2] discloses a redistribution layer [24] that comprises conductive lines [26,32] that redistribute bond pads [20c,20d] located on a right side and a left side of a first gap in an interior region to corresponding re-routed bond pads [28] in a periphery region. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Chia into the method of Kang to include a redistribution layer that comprises conductive lines that redistribute bond pads located on a right side and a left side of a first gap in an interior region to corresponding re-routed bond pads in a periphery region. The ordinary artisan would have been motivated to modify Kang in the manner set forth above for at least the purpose of redistributing the interconnect pattern on the die when the bond pads are not suitably placed [Kang; col.2 lines 36-40].

Regarding claims 54, 56-59, 65-66, and 68-69, Kang and Chia disclose wherein the step of electrically coupling is performed by wire bonding [Kang; 150 of Fig.1];

wherein the first die is identical in structure to the second die [Kang; 130₁ and 130₂ of Fig.1];

wherein the first and second dies comprise dynamic random access memory devices [Chia; para.66 lines 5-8];

wherein the first and second dies comprise double-data rate dynamic random access memory devices, each memory device including at least 512 Mb of memory cells [Both Kang and Chia disclose methods as applied to memory devices. It would be obvious that the memory devices would include dies that comprise double-data rate dynamic random access memory devices, each memory device including at least 512 Mb of memory cells.];

wherein, for both the first and second dies, the bond pads are positioned in a left column and a right column running parallel to a center line through the interior region, each bond pad in the left column being located to the left of the center line and each bond pad in the right column being located to the right of the center line, wherein the redistribution layer routes a plurality of bond pads from the right column across the center line to corresponding re-routed bond pads on the left side of the semiconductor device and also routes a plurality of bond pads from the left column across the center line to corresponding re-routed bond pads on the right side of the semiconductor device [Chia; Fig.2];

wherein, for both the first and second dies, the re-routed bond pads comprise elongated bond pads extending from an edge of the die toward the interior region of the die, wherein electrically coupling wire leads comprises: for the first die, attaching wires

to the re-routed bond pads at a portion of the re-routed bond pads nearer the edge of the first die; and for the second die, attaching wires to the re-routed bond pads at a portion of the re-routed bond pad nearer the interior region of the second die [Kang, col.2 lines 27-28, discloses the stacked dies can each be an integrated circuit or chip; it is obvious that it could include devices with various bond pad arrangements with redistribution trace and pad locations where wire bonding can take place.];

wherein the redistribution layer of the first and second dies comprise a multi-layer [36a-c] structure [Chia; Fig.9];

wherein the first die and the second die are both formed on a silicon substrate [Kang; col.2 lines 20-22] and wherein the spacer comprises a silicon spacer [Kang; col.3 lines 8-10];

wherein the substrate [110] includes at least one wiring layer formed inside the substrate, the wiring layer electrically coupling the contact pads [125] to conductive balls [125] on a second surface of the substrate [Kang; Fig.1].

3. Claims 55 and 70-72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang (U.S. Pat. 6943294) in view of Chia (U.S. Pub. 2003/0227079) as applied to claims 53-54 above, and further in view of Lo (U.S. Pub. 2003/0160312).

Kang and Chia fail to explicitly disclose the limitations of claims 55 and 70-72. However, Lo discloses

wherein the wire bonding is performed further to the interior of the second [18] die relative to the bonding of the first [12] die [Fig.1];

wherein placing the first die over the substrate comprises adhering the first die to the substrate with tape [Para.33 lines 7-11];

wherein placing the first die over the substrate comprises printing an adhesive over the substrate and placing the first die in the adhesive [Para.33 lines 7-11];

wherein electrically coupling wire leads from the re-routed bond pads of the first die and the second die to contacts formed in the substrate comprises electrically coupling wire leads from the re-routed bond pads of the first die [Step 142] before placing a spacer over the first die [Step 144] and electrically coupling wire leads from the re-routed bond pads of the second die [Step 150] after placing the second die over the spacer [Fig.5].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Lo into the method of Kang and Chia to include the limitations of claims 55 and 70-72. The ordinary artisan would have been motivated to modify Kang and Chia in the manner set forth above for at least the purpose of effectively stacking different sized dies.

4. Claims 60-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang (U.S. Pat. 6943294) in view of Chia (U.S. Pub. 2003/0227079) as applied to claims 53 and 56 above, and further in view of Itoh (U.S. Pat. 4439841).

Kang and Chia fail to explicitly disclose the limitations of claims 60-64. However, Itoh [Figs.1-4] discloses a method

wherein the redistribution layer of each of first and second dies includes a ground plane, the ground plane including a line [7,7',7'',7'''] substantially encircling the re-routed bond pads and a plurality ground lines that surround some of the re-routing lines;

wherein a plurality of the bond pads comprise data input/output bond pads, wherein the plurality ground lines [7,7',7'',7'''] surround some but not all of the re-routing lines, and wherein the plurality ground lines surround re-routing lines that are electrically coupled to the data input/output bond pads;

wherein the redistribution layer of the first die includes a first ground plane and wherein the redistribution layer of the second die includes a second ground plane [This is obvious];

wherein the first ground plane and the second ground plane each comprise ground lines [7,7',7'',7'''] adjacent a left side and a right side of a plurality of the conductive lines.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Itoh into the method of Kang and Chia to include the limitations of claims 60-64. The ordinary artisan would have been motivated to modify Kang and Chia in the manner set forth above for at least the purpose of improving memory device circuitry with increased signal transmission speed [Itoh; col.2 lines 19-22].

5. Claim 67 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang (U.S. Pat. 6943294) in view of Chia (U.S. Pub. 2003/0227079) as applied to claims 53 and 66 above, and further in view of Lin (U.S. Pub. 2004/0126927).

Kang and Chia fail to explicitly disclose the limitations of claim 67. However, Lin [Fig.44] discloses a method wherein redistribution layer [640] comprises: a titanium layer; a copper layer formed on the titanium layer; a nickel layer formed on the copper layer; and a gold layer formed on the nickel layer [Para.79 lines 11-17]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Lin into the method of Kang and Chia to include wherein redistribution layer comprises: a titanium layer; a copper layer formed on the titanium layer; a nickel layer formed on the copper layer; and a gold layer formed on the nickel layer. The ordinary artisan would have been motivated to modify Kang and Chia in the manner set forth above for at least the purpose of providing improved metallization contacts to enhance assemble reliability [Lin; para.12 lines 1-2].

6. Claims 73-78, 84-85, and 87-91 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang (U.S. Pat. 6943294) in view of Chia (U.S. Pub. 2003/0227079) and Lo (U.S. Pub. 2003/0160312).

Regarding claim 73, Kang and Chia disclose most of the limitations as discussed above in claim 53. Kang and Chia fail to explicitly disclose wherein the first die is a different size than the second die and the second die is positioned on the first die such that the re-routed bond pads of the first die are not covered by the second die.

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However, Lo [Fig.1] discloses a method wherein the first die [12] is a different size than the second die [18] and the second die is positioned on the first die such that the re-routed bond pads of the first die are not covered by the second die. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Lo into the method of Kang and Chia to include wherein the first die is a different size than the second die and the second die is positioned on the first die such that the re-routed bond pads of the first die are not covered by the second die. The ordinary artisan would have been motivated to modify Kang and Chia in the manner set forth above for at least the purpose of effectively stacking different sized dies.

Kang, Chia, and Lo disclose the limitations of claims 74-78, 84-85, and 87-91 as previously discussed above in the rejection of claims 53-59, 65-66, and 68-72.

Claims 79-83 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang (U.S. Pat. 6943294) in view of Chia (U.S. Pub. 2003/0227079) and Lo (U.S. Pub. 2003/0160312) and further in view of Itoh (U.S. Pat. 4439841).

Kang, Chia, Lo, and Ito disclose the limitations of claims 79-83 as previously discussed above in the rejection of claims 60-64.

Claim 86 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang (U.S. Pat. 6943294) in view of Chia (U.S. Pub. 2003/0227079) and Lo (U.S. Pub. 2003/0160312) and further in view of Lin (U.S. Pub. 2004/0126927).

Kang, Chia, Lo, and Lin disclose the limitations of claim 86 as previously discussed above in the rejection of claims 67.

7. Claims 92-93, 95-98, 104-105, and 107-108 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang (U.S. Pat. 6943294) in view of Chia (U.S. Pub. 2003/0227079).

Regarding claim 92, Kang [Fig.1] discloses a method of forming a stacked-die assembly, the method comprising:

- providing a substrate [110] with contacts [125] formed on a top surface;
- placing a bottom side of a first die [130₁] over the top surface of the substrate;
- placing a spacer over the first die [140₁];
- placing a bottom side of a second die [130₂] over the spacer; and
- electrically coupling wire leads [150] from the re-routed bond pads [145] of the first die and the second die to the contacts.

Kang [Col.2 lines 36-40] discloses a redistribution layer wherein each of the first die and second die comprises re-routing lines that redistribute bond pads, but fails to explicitly disclose a redistribution layer that comprises re-routing lines that redistribute bond pads located on a right side of a first gap to re-routed bond pads in a periphery region along a left side and re-routing lines that redistribute bond pads located on a left side of a first gap to re-routed bond pads in a periphery region along a right side.

However, Chia [Fig.2] discloses a redistribution layer [24] that comprises re-routing lines [32] that redistribute bond pads [20c,20d] located on a right side of a first

gap to re-routed bond pads in a periphery region along a left side and re-routing lines that redistribute bond pads located on a left side of a first gap to re-routed bond pads in a periphery region along a right side. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Chia into the method of Kang to include the limitation of the claim. The ordinary artisan would have been motivated to modify Kang in the manner set forth above for at least the purpose of redistributing the interconnect pattern on the die when the bond pads are not suitably placed [Kang; col.2 lines 36-40].

Regarding claims 93, 95-98, 104-105, and 107-108, Kang and Chia disclose the limitations of these claims as previously discussed above in the rejection of claims 54, 56-59, 65-66, and 68-69.

Claims 94 and 109-111 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang (U.S. Pat. 6943294) in view of Chia (U.S. Pub. 2003/0227079) as applied to claims 92-93 above, and further in view of Lo (U.S. Pub. 2003/0160312).

Kang, Chia, and Lo disclose the limitations of claims 94 and 109-111 as previously discussed above in the rejection of claims 55 and 70-72.

Claims 99-103 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang (U.S. Pat. 6943294) in view of Chia (U.S. Pub. 2003/0227079) as applied to claims 92 and 95 above, and further in view of Itoh (U.S. Pat. 4439841).

Kang, Chia, and Ito disclose the limitations of claims 99-103 as previously discussed above in the rejection of claims 60-64.

Claim 106 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang (U.S. Pat. 6943294) in view of Chia (U.S. Pub. 2003/0227079) as applied to claims 92 and 105 above, and further in view of Lin (U.S. Pub. 2004/0126927).

Kang, Chia, and Lin disclose the limitations of claim 106 as previously discussed above in the rejection of claims 67.

Response to Arguments

8. Applicant's arguments filed October 2, 2006 have been fully considered but they are not persuasive. Applicant argues that Chia discloses interconnecting bond pads across adjacent dies which is in contrast to Applicant's claimed limitation of a redistribution layer "that comprises conductive lines that redistribute bond pads located on a right side and a left side of a first gap in an interior region to corresponding re-routed bond pads in a periphery region" being on each die. This argument is not persuasive. Firstly, the claim is not so limited wherein die is defined to exclude the chip package 10 of Chia. As disclosed in Figs.1-2 of Chia, chip package 10 is a singulated package from an entire wafer. It is not meant to be further divided. Chip package 10 can be interpreted as a die with different die regions, 12a-d, analogous to Applicant's Fig.2b. Additionally, Fig.4 of Chia, for example, discloses wherein continuous films 22 and then 24 are deposited onto the die surface. As depicted, substrate 14 can be

accurately interpreted as a semiconductor die with regions 12c and 12d, rather than being separate devices. Consequently, structure 10 can be interpreted as a large single die. Overall, arguments are not persuasive and the rejection is maintained.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Heng (U.S. Pub. 2005/0045378) discloses, in Fig.5, a redistribution layer that comprises conductive lines that redistribute bond pads located on a right side and a left side of a first gap in an interior region to corresponding re-routed bond pads in a periphery region on each die.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

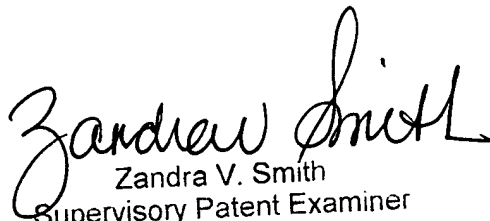
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bac H. Au whose telephone number is 571-272-8795. The examiner can normally be reached on Mon-Fri 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BHA


Zandra V. Smith
Supervisory Patent Examiner
12 Jan 2007